In the Claims:

1. (Original) A phase-changeable memory device, comprising:

a substrate;

an access transistor formed in and/or on the substrate;

laterally spaced apart first and second conductive patterns disposed on the substrate and having opposing sidewalls;

a conductor electrically connecting the first conductive pattern to a source/drain region of the access transistor; and

a phase-changeable material region disposed between the first and second conductive patterns and contacting the opposing sidewalls of the first and second conductive patterns.

2. (Original) A memory device according to Claim 1:

wherein the access transistor comprises:

first and second source/drain regions in the substrate; and

a gate electrode disposed on the substrate between the first and second source drain regions;

wherein the memory device further comprises an insulating layer disposed on the substrate and overlying the gate electrode and the first and second source/drain regions;

wherein the first and second conductive patterns are disposed on the insulating layer;

wherein the conductor passes through the insulating layer and connects the first conductive pattern to the first source/drain region; and

wherein the phase-changeable material layer is disposed on the insulating layer between the first and second conductive patterns.

3. (Original) A memory device according to Claim 2, wherein the first and second conductive patterns overlie respective ones of the first and second

source/drain regions, and wherein the phase-changeable material region overlies the gate electrode.

4. (Original) A memory device according to Claim 3, wherein the conductor extends from the first source/drain region to contact the overlying first conductive pattern at a first contact area, and wherein the first conductive pattern contacts the phase-changeable material region at a second contact area that is substantially smaller than the first contact area.

5. (Original) A memory device according to Claim 4:

wherein the insulating layer comprises a first insulating layer;

wherein the conductor comprises a first conductor, and wherein the memory device further comprises:

a second insulating layer disposed on the substrate and overlying the first and second conductive patterns; and

a second conductor passing through the second insulating layer and contacting the second conductive pattern at a third contact area; and

wherein the second conductive pattern contacts the phase-changeable material region at a fourth contact area that is substantially smaller than the third contact area.

6. (Original) A memory device according to Claim 5, wherein each of the first and second conductive patterns comprises a body portion that contacts the corresponding one of the first and second conductors and a smaller tab portion that extends from the body portion to contact the phase-changeable material region.

7. (Original) A memory device according to Claim 5, further comprising:

a bit line conductor disposed on the second insulating layer, wherein the second conductor electrically connects the second conductive pattern to the bit line conductor;

a common drain line conductor disposed in the first insulating layer between the second conductive pattern and the second source/drain region; and

a third conductor extending from the second source/drain region to contact the common drain line conductor.

8. (Original) A memory device according to Claim 1, wherein the phase-changeable material layer comprises a material having a resistivity that is dependent upon a phase of the phase-changeable material region.

9. (Original) A memory device according to Claim 8, wherein the phase-changeable material layer comprises a compound of germanium (Ge), stibium (Sb) and tellurium (Te).

10. (Original) A phase-changeable memory cell, comprising:

first and second spaced apart conductive patterns having opposing sidewalls; and

a phase-changeable material region disposed between the first and second conductive patterns and contacting the opposing sidewalls thereof.

11. (Original) A memory cell according to Claim 1, wherein each of the first and second conductive patterns comprise:

a body portion configured to contact a conductor at a first contact area;

a tab portion extending from the body portion to contact the phase-changeable material region at a second contact area that is perpendicular to the first contact area and that is substantially smaller than the first contact area.

12. (Original) A phase-changeable memory device structure comprising:

a pair of conductive patterns spaced apart from each other on the same plane;

a variable resistor pattern disposed between the pair of conductive patterns so as to be in direct contact with opposing sidewalls of the conductive patterns at active contact areas;

an upper metal interconnection disposed over the conductive patterns and the variable resistor pattern, wherein the upper metal interconnection is electrically connected to one conductive pattern; and

a semiconductor substrate disposed below the conductive patterns and the variable resistor pattern, wherein the semiconductor substrate has an impurity diffusion region that is electrically connected to the other conductive pattern.

13. (Original) The structure as claimed in claim 12, wherein the variable resistor pattern includes a phase-changeable material.

14. (Original) The structure as claimed in claim 12, wherein the upper metal interconnection is electrically connected to one conductive pattern through an upper contact plug penetrating an upper insulating layer disposed on the conductive patterns and the variable resistor pattern,

wherein the impurity diffusion region is electrically connected to the other conductive pattern through a lower contact plug penetrating a lower insulating layer disposed under the conductive patterns and the variable resistor pattern.

15. (Original) The structure as claimed in claim 14, further comprising:

another impurity diffusion region spaced apart from the impurity diffusion region in the semiconductor substrate;

a gate line disposed on a semiconductor substrate between the impurity diffusion region and the other impurity diffusion region, and in the lower insulating layer; and

a common drain electrode disposed in the lower insulating layer, wherein the common drain electrode is electrically connected to the other impurity diffusion region through a predetermined region of the lower insulating layer.

16. (Original) The structure as claimed in claim 12, wherein a crystallization structure of a variable resistor material constituting the active contact areas is changed depending on density of currents flowing across the active contact area of the variable resistor pattern.

17. (Original) The structure as claimed in claim 15, wherein when current flows between the upper metal interconnection and the common drain electrode a crystallization structure of a variable resistor material constituting the active contact areas is changed depending on density of currents flowing across the active contact area of the variable resistor pattern.

18. (Original) The structure as claimed in claim 12, wherein the pair of conductive patterns includes titanium nitride.

19. (Original) The structure as claimed in claim 12, wherein the lower contact plug and the upper contact plug include respectively titanium, titanium nitride, and tungsten that are sequentially stacked.

20. (Original) A phase-changeable memory device structure comprising:

a phase-changeable material pattern having active contact areas at both sides thereof;

a pair of conductive patterns disposed symmetrically on the same plane as the phase-changeable material pattern, wherein the conductive patterns are in direct contact with the active contact areas of the phase-changeable material pattern;

an upper insulating layer disposed on the phase-changeable material pattern and the conductive patterns;

a bit line disposed on the upper insulating layer, wherein the bit line is electrically connected to one conductive pattern through an upper contact plug penetrating the upper insulating layer;

a lower insulating layer disposed under the phase-changeable material pattern and the conductive patterns; and

a semiconductor substrate having a source region electrically connected to the other conductive pattern through a lower contact plug penetrating the lower insulating layer.

21. (Original) The structure as claimed in claim 20, further comprising:

a drain region spaced apart from the source region to be formed in the semiconductor substrate;

a gate line disposed on a semiconductor substrate between the source and drain regions; and

a common drain electrode disposed in the lower insulating layer, wherein the common drain electrode is electrically connected to the drain region through a predetermined region of the lower insulating layer.

22. (Original) The structure as claimed in claim 20, wherein the conductive pattern includes titanium nitride.

23. (Original) The structure as claimed in claim 21, wherein a crystallization structure of a phase-changeable material constituting the active contact areas is changed depending on density of currents flowing across the active contact areas of the variable resistor pattern, so that resistivity of the active contact areas is varied.

24. (Original) A phase-changeable memory device structure comprising:

a phase-changeable material pattern having active contact areas at both sides thereof;

a first electrode pattern disposed on the same plane as the phase-changeable material pattern, wherein the first electrode pattern is in contact with one active contact area;

a second electrode pattern disposed on the same plane as the phase-changeable material pattern, wherein the second electrode pattern is in contact with the other active contact area;

a resistance detection interconnection electrically connected to the second electrode interconnection; and

a semiconductor substrate including an impurity diffusion region electrically connected to the first electrode interconnection.

25. (Original) The structure as claimed in claim 24, wherein an upper insulating layer is interposed between the phase-changeable material pattern and the resistance detection interconnection and between the electrode patterns and the resistance detection interconnection, and the resistance detection interconnection is electrically connected to the second electrode pattern through an upper contact plug penetrating the upper insulating layer,

wherein a lower insulating layer is interposed between the phase-changeable material pattern and the semiconductor substrate and between the electrode patterns and the semiconductor substrate, and the impurity diffusion region is electrically connected to the first electrode pattern through a lower contact plug penetrating the lower insulating layer.

26. (Original) The structure as claimed in claim 25, wherein each electrode pattern includes a plug contact region contacting with a contact plug and a material pattern contact region protruding from a middle portion of sidewalls of the plug contact region toward the phase-changeable material pattern to be in contact with the active contact area.

27. (Original) The structure as claimed in claim 26, wherein dimensions of the active contact area is determined according to a thickness and a width of the material pattern contact region.

28. (Original) The structure as claimed in claim 27, wherein the width of the material pattern contact region is less than the thickness thereof.

29.-45. (Cancelled)